EXPRESS MAIL LABEL NO.: EV 264256993 US

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 121(c)(ii)

1. (Twice Amended) A processor comprising:

a register file; and

a functional unit, coupled to the register file, that executes an instruction that operates upon plural registers of said register file, including at least one register explicitly identified by a**n explicitly defined** register specifier and at least one other register implicitly identified by the **explicitly-defined** register specifier.

3. (Amended) A processor according to Claim 1 wherein:

[the] a register specifier **for the other register** is implicitly derived by adding one to **[an] the** explicitly-defined register specifier.

6. (Amended) A processor according to Claim 1 wherein:

the instruction is a bit extract instruction that uses an implicitly-derived register specifiers and has a form of:

bitext rsl, rs2, rd,

and per.forms an operation of extracting bits from even-aligned pairs of registers r[rsl] and [rsl+ 1] where the term [rsl+l] designates data contained within the **other** register following the explicitly-defined register rsl, wherein data in register r[rs2] describes the extracted field of registers r[rsl] and r[rsl + 1] and register r[rd] is a destination register.

11. (Amended) A processor according to Claim 1 wherein:

the instruction is a double-precision floating point subtraction instruction that uses an implicitly-derived register specifiers and has a form of:

dsub rsl, rs2, rd,

and performs an operation specified by the equation:

(rd, [rd+l]) = (rsl, [rsl+l]) - (rs2, [rs2+1]),

where the terms (rsl, [rsl+l]), (rs2, [rs2+1]), and (rd, [rd+1]) designate double-precision words.

17.(Amended) A processor according to Claim 1 **further comprising:**

[wherein said decoder is generating] **a decoder coupled to the functional unit and configured to generate** a first pointer pointing to the explicitly-specified register and a second pointer pointing to the **other** **[implicitly-derived]** register.

19.(Amended) A processor according to Claim 1 further comprising:

a pointer coupled to the register file and designating a register in the register file, the pointer including a signal indicative of selection of a **the other** **[implicitly-derived]** register, wherein a register read of the explicitly-specified register is accompanied by a register read of the **[implicitly-derived]** **other** register when implicit derivation of **[a]** **the explicitly-defined** register specifier is selected.

20. (Twice Amended) A method of operating a processor comprising:

storing information in a register file including a plurality of registers;

executing instructions in a functional unit coupled to the register file and operating upon a plurality of registers in the register file;

explicitly defining a register specifier of a register operated upon during executing of the instruction; and

implicitly deriving a register specifier of **[a]** **at least one other** register operated upon during executing of the instruction based on the explicitly defined register specifier.

21. (Amended) A method according to Claim 20 further comprising:

decoding an instruction; and

deriving, during decoding of the instruction, a register specifier based on **[an]** **the** explicitly-specified register specifier of the instruction.

24. (New) A method according to Claim 20 further comprising:

implicitly deriving the register specifier for the other register by adding one to the explicitly-defined register specifier.